



Static Timing Analysis for Nanometer Designs: A Practical Approach

J. Bhasker, Rakesh Chadha

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Timing, timing, timing! That is the main concern of a digital designer charged with designing a semiconductor chip. What is it, how is it described, and how does one verify it? The design team of a large digital design may spend months architecting and iterating the design to achieve the required timing target. Besides functional verification, the timing closure is the major milestone which dictates when a chip can be released to the semiconductor foundry for fabrication. This book addresses the timing verification using static timing analysis for nanometer designs. The book has originated from many years of our working in the area of timing verification for complex nanometer designs. We have come across many design engineers trying to learn the background and various aspects of static timing analysis. Unfortunately, there is no book currently available that can be used by a working engineer to get acquainted with the details of static timing analysis. The chip designers lack a central reference for information on timing, that covers the basics to the advanced timing verification procedures and techniques.

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